

REMARKS/ARGUMENTS

Claims 1-11 are pending in this application, and claims 1-11 stand rejected. Applicants have amended claims 1-4, 6-7, 9 and 10 to improve the use of idiomatic English and, to make explicit what was implicit in these claims. These amendments do not in any way narrow the scope of the claims as filed. We have attached a marked-up version showing the changes made to the claims. The attachment is captioned “Version with markings to show changes made.”

In light of these amendments and the remarks set forth below, Applicant respectfully submits that each of the pending claims is in immediate condition for allowance.

The Examiner rejected claim 1 as indefinite under 35 U.S.C. § 112 because the term “transmission circuit” was not defined. Examiner also rejected claim 2 under 35 U.S.C. § 112 because it depends from claim 1, and because “there is insufficient antecedent basis for the term ‘the shift size.’” In light of the Examiner’s remarks and to more clearly define the invention, Applicant has amended claims 1 and 2 and respectfully requests that the Examiner withdraw his rejection under 35 U.S.C. § 112.

The Examiner rejected claims 1, 3, 6, and 9 as unpatentable under 35 U.S.C. § 103(a) for being obvious over U.S. Patent No. 6,052,383 (“Stoner”) in view of U.S. Patent No. (“5,278,828 (“Chao”). The Examiner’s rejection is respectfully traversed.

To establish a prima facie case of obviousness, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify a reference or combine references to arrive at the claimed subject matter. The prior art references must also teach or suggest all the limitations of the claim in question. See MPEP § 706.02(j).

The combination of Stoner and Chao does not teach or suggest all the limitations of claims 1, 3, 6, and 9. Among the limitations of these claims neither taught nor suggested by Stoner and Chao is the requirement of writing a frame-relay frame to a memory location “shifted from an end of the next available memory location in the frame buffer.”

Moreover, the Examiner fails to point to any suggestion or motivation in either Stoner or Chao, or in knowledge generally available to one of ordinary skill in the art, for writing a frame-relay frame to an address shifted from the top available address of a frame buffer in a memory to achieve the particular advantages described in Applicant’s specification and figures. As a result, claims 1, 3, 6 and 9 are not obvious over Stoner in light of Chao and should be allowed.

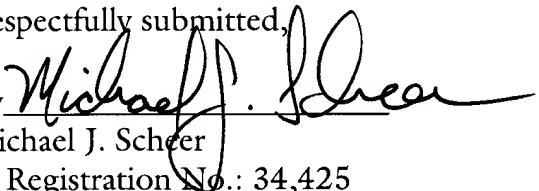
The Examiner also rejected claims 2, 4-5, 7, 10-11 as unpatentable over Stoner in view of Chao. Claims 2, 4-5, 7 and 10-11 depend from, and contain all of the limitations of, claims 1, 3, 6 and 9, respectively. These claims also recite additional limitations which, in combination with the limitations of claims 1, 3, 6 and 9, are neither disclosed nor suggested in the art of record and are also believed to be directed towards the patentable subject matter. As a result, Applicant submits that the rejection of claims 2, 4-5, 7, and 10-11 should also be withdrawn.

For the reasons stated above, Applicants believe that each of the pending claims in this application is in immediate condition for allowance. Accordingly, Applicants respectfully request that the Examiner withdraw the outstanding rejection of these claims and to pass this application to issue.

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Respectfully submitted,

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Version With Markings to Show Changes Made

1. (Amended) A frame-relay frame [transmission circuit] processing device for reassembling a frame-relay frame into an Asynchronous Transfer Mode (ATM) cell, wherein[,] said device receives a [when a received]frame-relay frame [is written in]and writes said frame to a memory location[, said frame is written from an address]shifted from [the top]an end of the next available memory location in the [of a]frame buffer.

2. (Amended) A frame-relay frame [transmission circuit]processing device according to claim 1, wherein a [the shift]size of the shift from an end of the next available memory location is determined for each connection.

3. (Amended) A [frame-relay] frame relay [transmission] circuit for reassembling a frame-relay frame into an Asynchronous Transfer Mode (ATM) cell comprising:

a processor for determining for each connection a size of a shift [size for each connection, said shift size]by which said frame is to be shifted from [the top]an end of the next available memory location in [address of]a frame buffer;

a frame receiver for receiving said frame through said connection;

a memory for storing said received frame [in a frame buffer from]at [an address]a location shifted from [the top of]an end of the next available memory location in the [a]frame buffer by said shift size; and

a segmentation and reassembling device for reassembling said frame into said ATM cell.

4. (Amended) A [frame-relay] frame relay [transmission] circuit according to claim 3, wherein, for each connection, said processor writes [the set of]a data link connection identifier (DLCI) and said shift size into a connection table, and retrieves said shift size [in]from said connection table using said DLCI as a key.

5. (Amended) A [frame-relay] frame relay [transmission] circuit according to claim 3, wherein said frame received by said frame receiver is transmitted to said memory through direct memory access.

6. (Amended) A method for reassembling a frame-relay frame into an Asynchronous Transfer Mode (ATM) cell comprising the steps of:

determining a shift size for each connection by which said frame is to be shifted from [the top]an end of the next available memory location [address of]in a frame buffer [in a memory];

receiving said frame and writing said frame starting from an address shifted [from the top address of said available area of said frame buffer]by said shift size; and

reassembling said frame into an ATM cell.

7. (Amended) A method according to claim 6, further comprising the steps of:

writing [a set of]a data link connection identifier (DLCI) and said shift size into a connection table for each connection; and

retrieving said shift size [in]from said connection table using said DLCI as a key.

9. (Amended) A computer readable medium containing program instructions for reassembling a frame-relay frame into an Asynchronous Transfer Mode (ATM) cell, the program instructions including instructions for performing the steps comprising:

determining a shift size for each connection by which said frame is to be shifted from [the top address]an end of the next available memory location in a [of]frame buffer [in a memory];

receiving said frame and writing said frame starting from an address shifted [from the top address of said frame buffer]by said shift size; and

reassembling said frame into an ATM cell.

10. (Amended) A computer readable medium according to claim 9, wherein said program instructions include instructions for:

writing a set of a data link connection identifier (DLCI) and said shift size into a connection table for each connection; and

retrieving said shift size in said connection table using said DLCI as a key.